Claim 1 is directed to a partial product bit generator circuit for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a digital signal having a plurality of bits, the multiplier being represented by a digital signal having a plurality of bits, the partial product bit generator circuit receiving a group of the multiplicand bits and a group of the multiplier bits and providing a partial product bit in response thereto. The partial product bit generator comprises less than six levels of combinatorial logic.

The Examiner asserts that equation (1) in Fig. 4A could be implemented in three levels of combinatorial logic and therefore reads on claim 1. This assertion is respectfully traversed. It appears the Examiner has mistakenly assumed that equation (1) corresponds to claim 1. However, equation (1) represents the partial product bit as a function of intermediate signals, whereas claim 1 defines the partial product bit as a function of multiplier bits and multiplicand bits.

The equations of Fig. 4A are repeated on page 4 of the specification. As explained therein, X_1, X_2, and N are intermediate signals (page 4, line 11). The intermediate signals X_1, X_2, and N are defined by equations (2)-(4), respectively, in terms of the multiplier bits. Thus, if the partial product bit PPj_i of equation (1) is expressed in terms of multiplicand bits and multiplier bits, a more complex expression is obtained. An implementation of the more complex expression is shown in Fig. 5A of the present application. A second implementation is shown in Fig. 5B of the present application. As explained at page 6, line 17 to page 7, line 10 of the present application, the implementation of Fig. 5A has six levels of combinatorial logic. As described therein, most logic gates include one level of combinatorial logic, except that an exclusive-or (XOR) gate includes two levels of combinatorial logic. Thus, the prior art implementations of Figs. 5A and 5B have six levels of combinatorial logic between multiplier bits b and partial product bit PPj_i.

In summary, the cited passages of the present application describe partial product bit generator circuits having six levels of combinatorial logic and do not anticipate claim 1, which is directed to a partial product bit generator circuit having *less* than six levels of combinatorial logic. Accordingly, claim 1 is clearly and patentably distinguished over the cited passages of the present application, and withdrawal of the rejection is respectfully requested.

Claims 6-8 depend from claim 1 and are patentable over the cited reference for at least the same reasons.

Claim 10 is directed to a method for use in performing multiplication to generate a product of a multiplicand and a multiplier and requires, in part, generating a partial product bit signal in response to a group of multiplicand bits and a group of multiplier bits using less than six levels of combinatorial logic. Claim 10 is patentable over the cited reference for at least the reasons discussed above in connection with claim 1. Accordingly withdrawal of the rejection of claim 10 is respectfully requested.

Claims 12-14 depend from claim 10 and are patentable over the cited reference for at least the reasons discussed above in connection with claims 1 and 10.

Claim 15 is directed to a partial product bit generator circuit for use in performing multiplication to generate a product of a multiplicand and a multiplier and requires, in part, means for generating a partial product bit signal in response to a group of multiplicand bits and a group of multiplier bits using less than six levels of combinatorial logic. Claim 15 is patentable over the cited reference for at least the reasons discussed above in connection with claims 1 and 10.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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